

FIG. 1

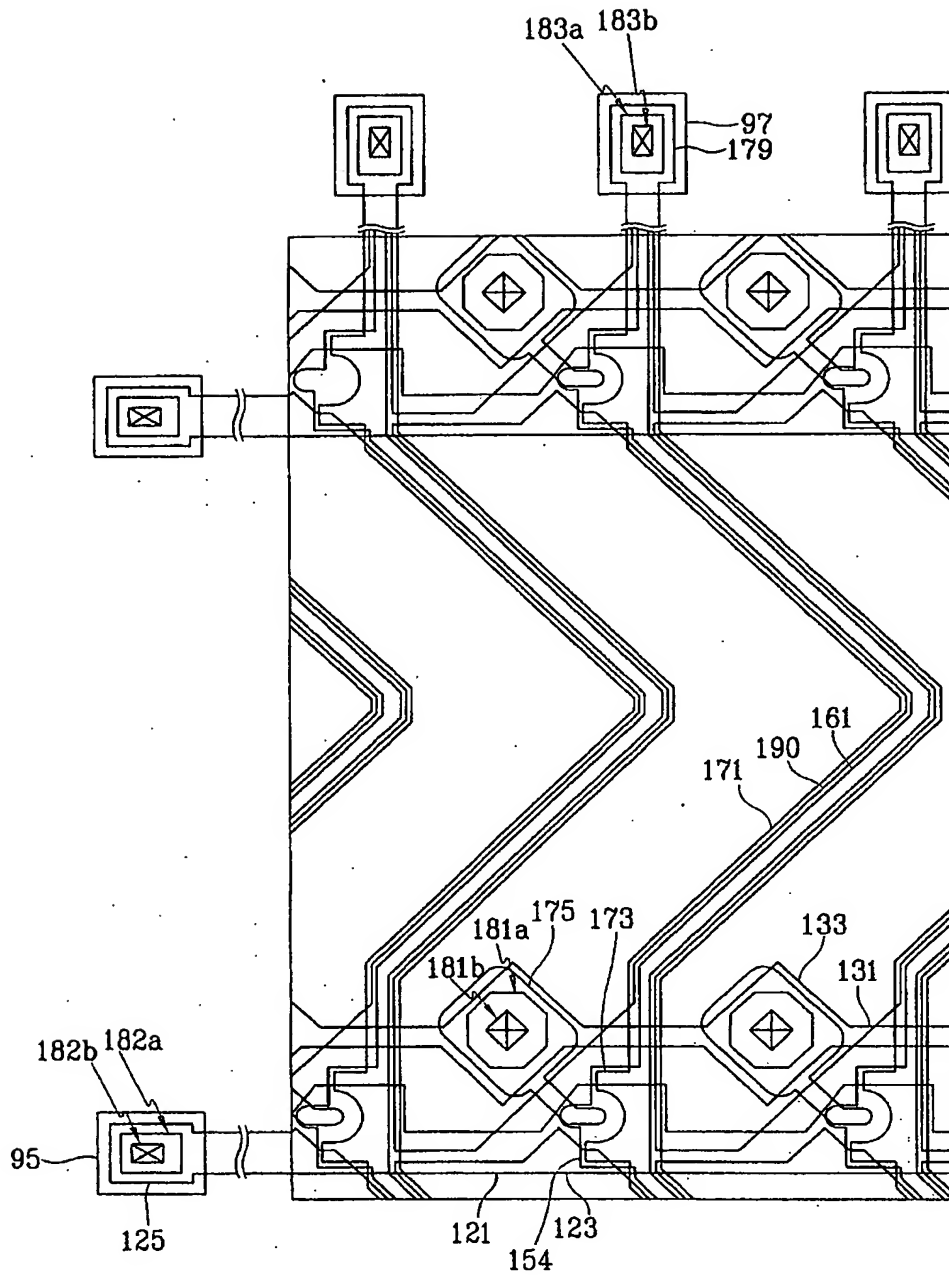


FIG.2

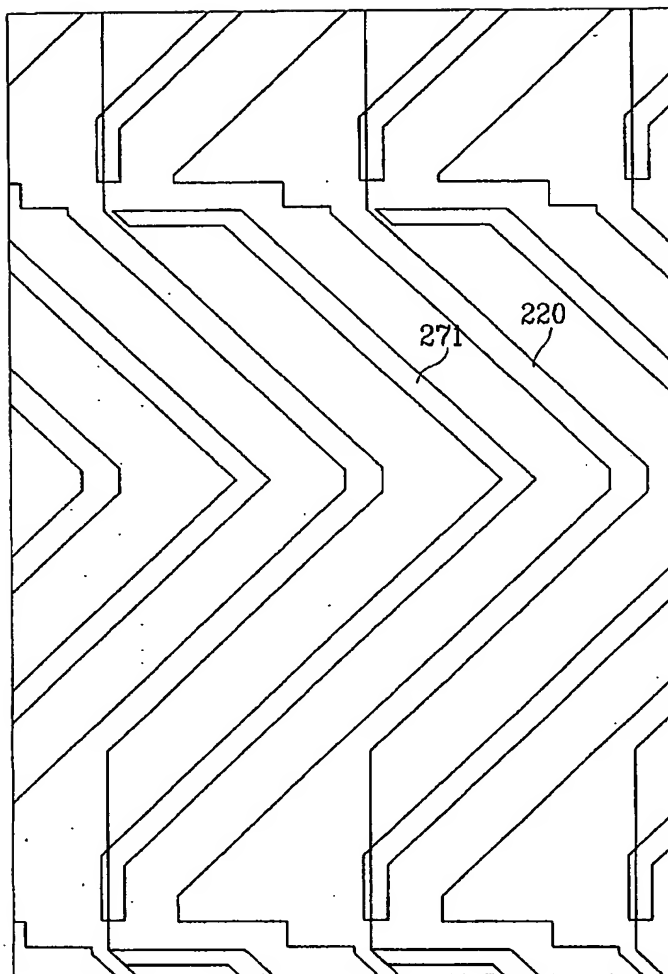


FIG.3

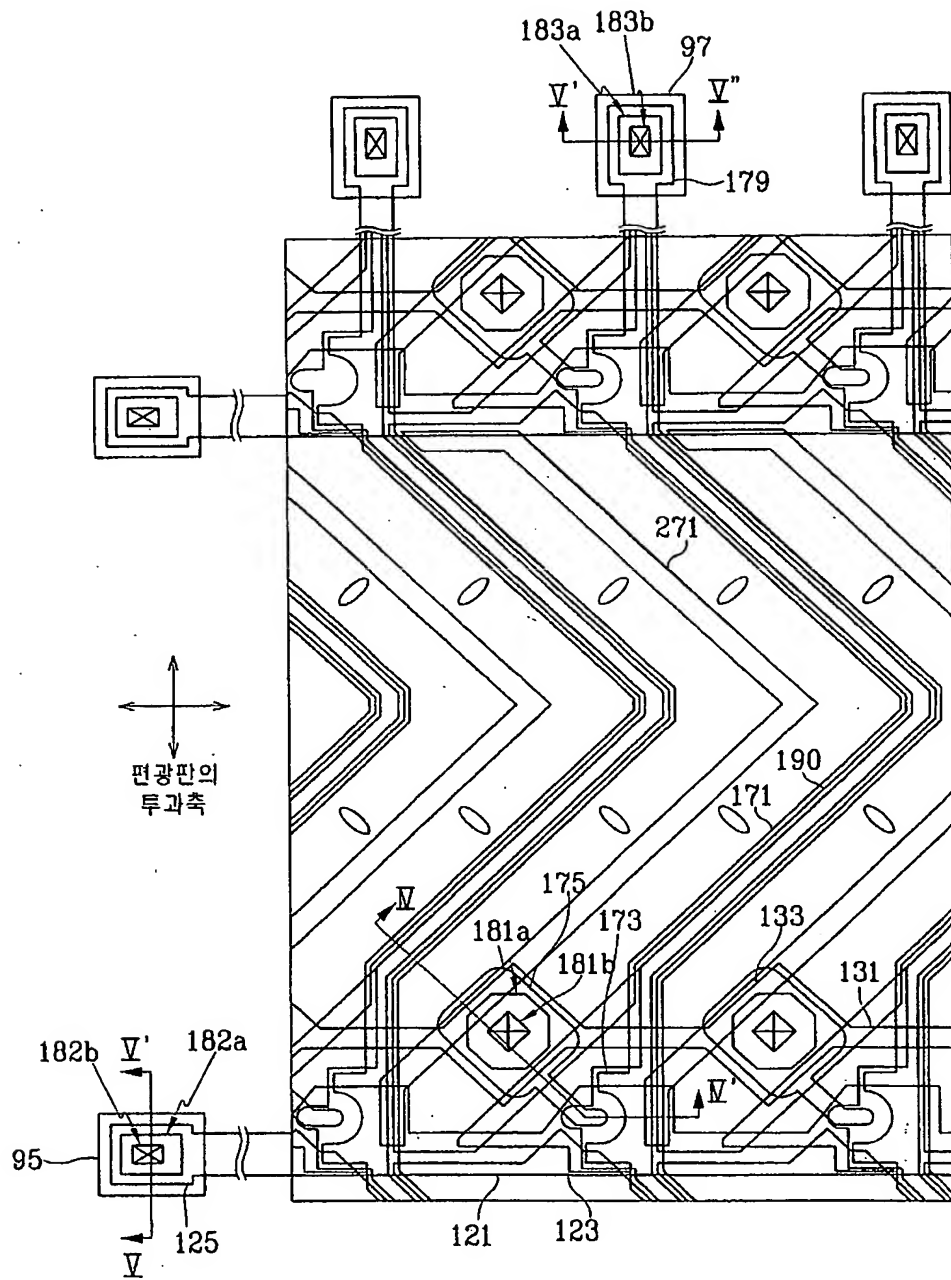


FIG.4

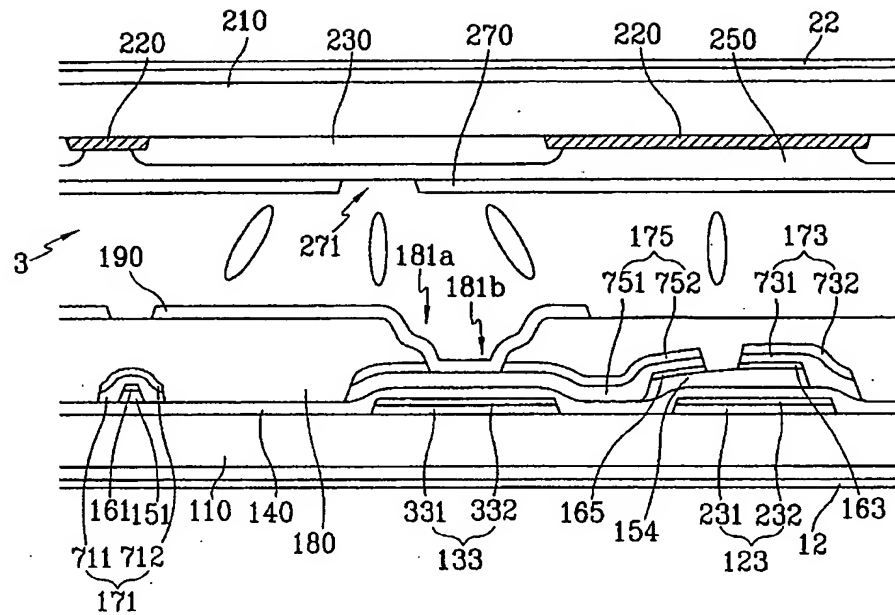


FIG.5

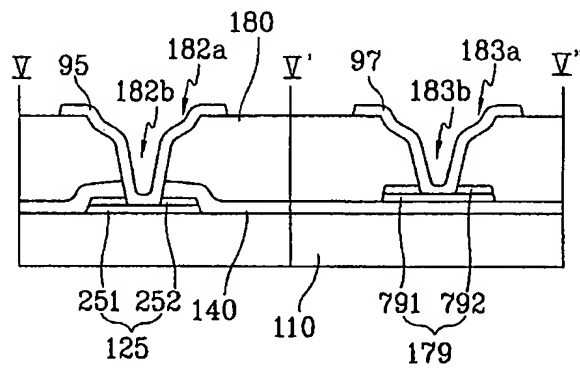


FIG.6A

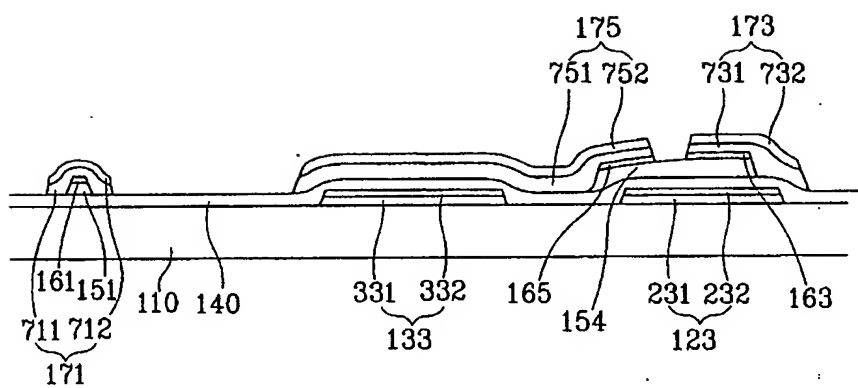


FIG.6B

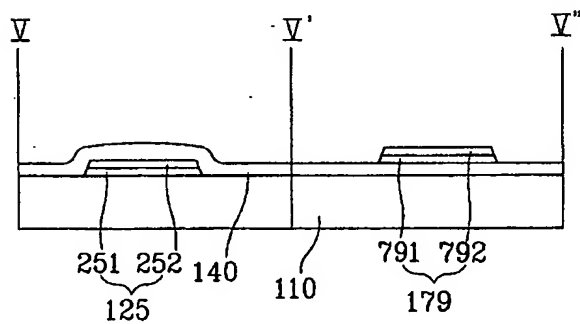


FIG.7A

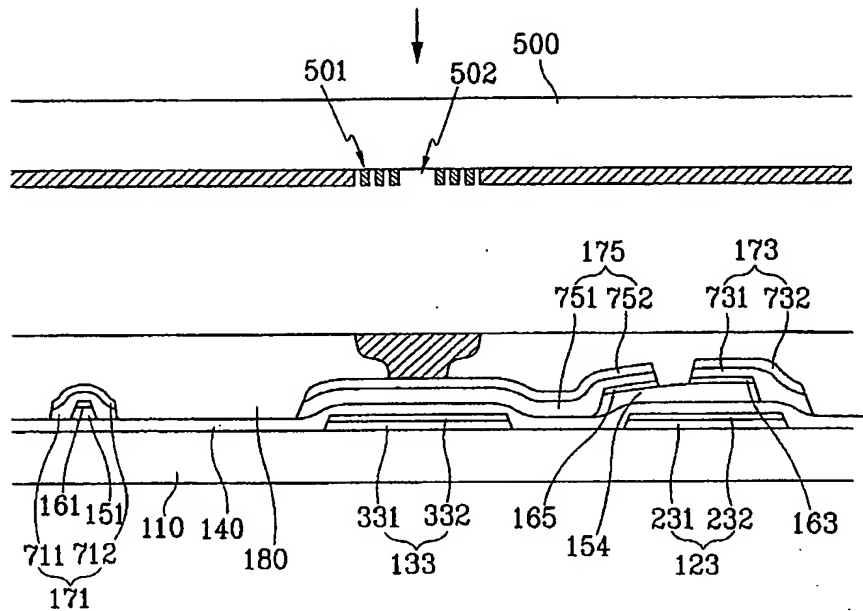


FIG.7B

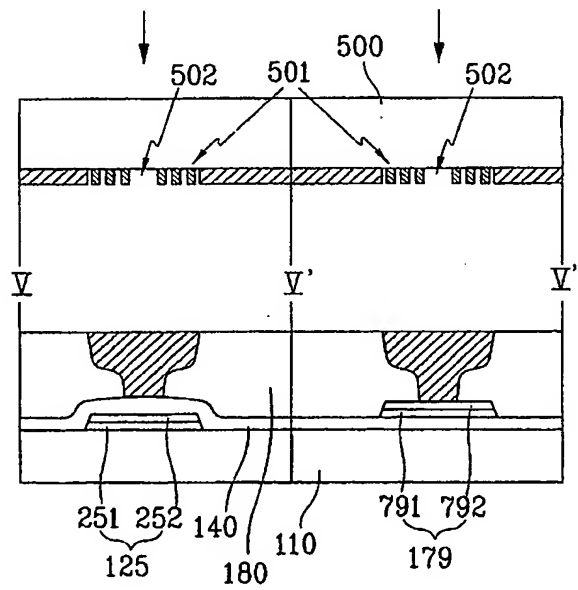
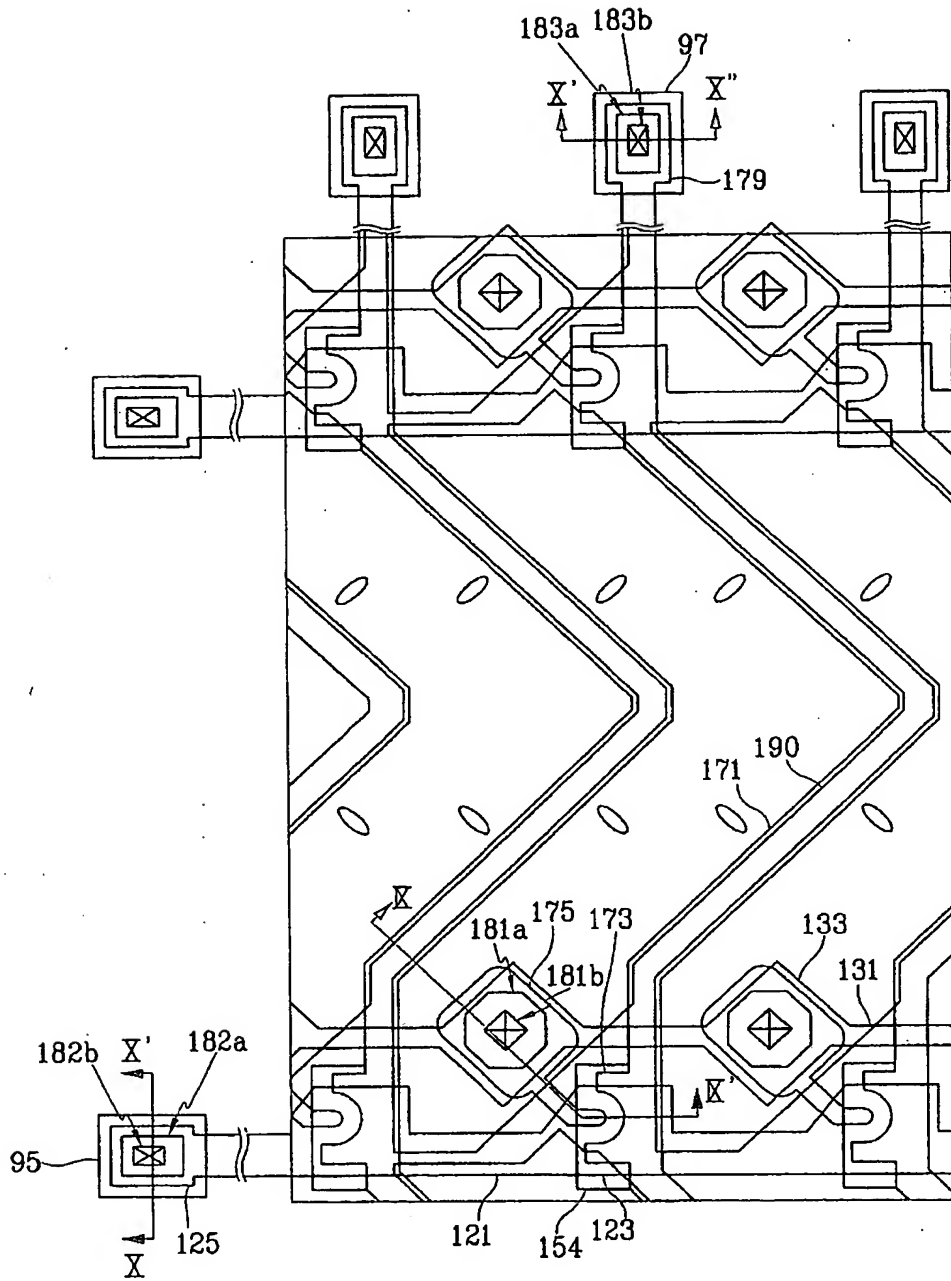


FIG.8



[illegible]

This cross-sectional view shows a semiconductor device with two gate structures. The left gate structure (180) has a gate stack (182a, 182b) on a gate dielectric (180). Below it is a channel region (140) with source/drain regions (251, 252) and a buried layer (125). The right gate structure (97) has a gate stack (183a, 183b) on a gate dielectric (97). Below it is a channel region (151) with source/drain regions (791, 792) and a buried layer (179). A common layer (110) is at the bottom. Cross-sections X-X' and X'' are indicated.



FIG.11A

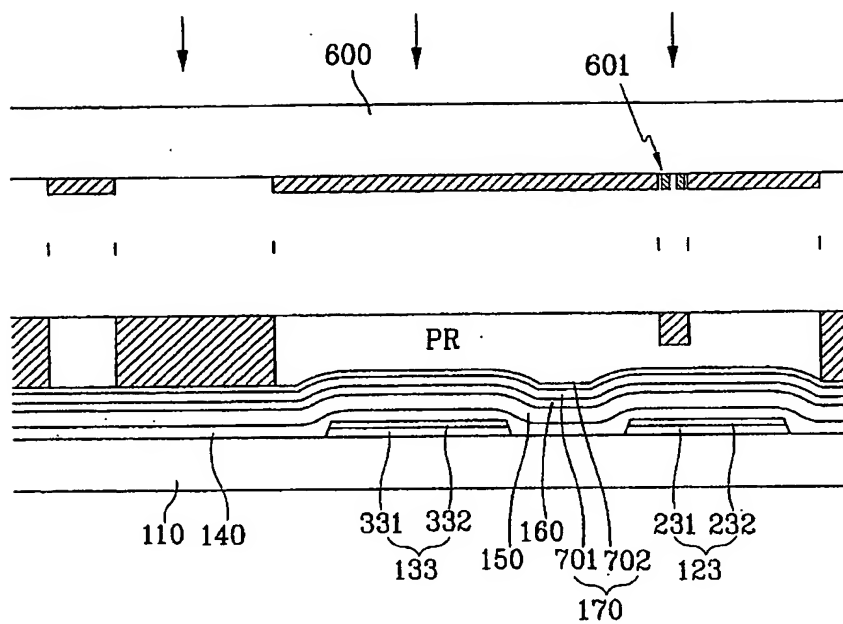


FIG.11B

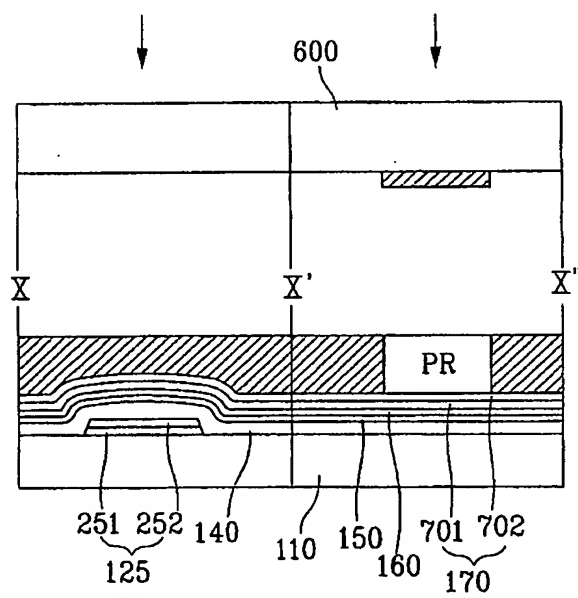


FIG.12A

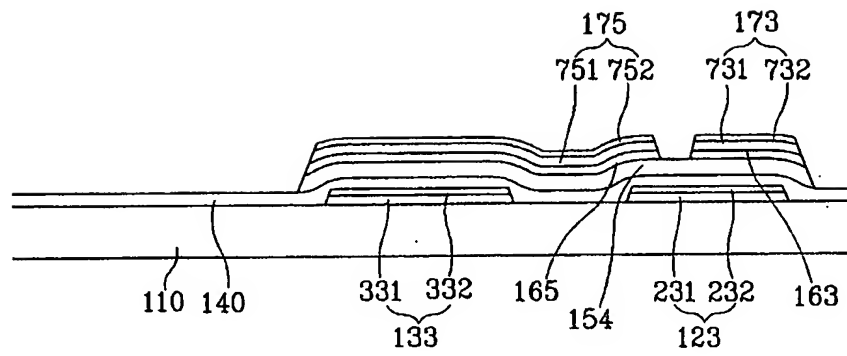


FIG.12B

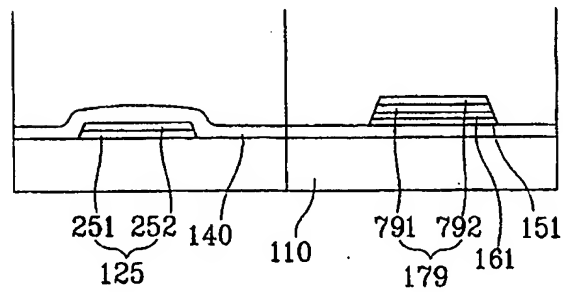


FIG.13A

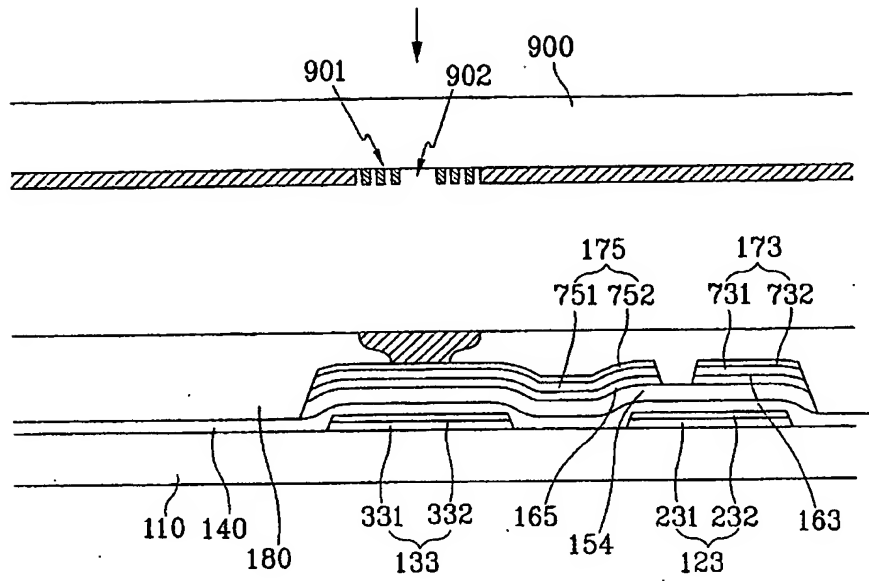


FIG.13B

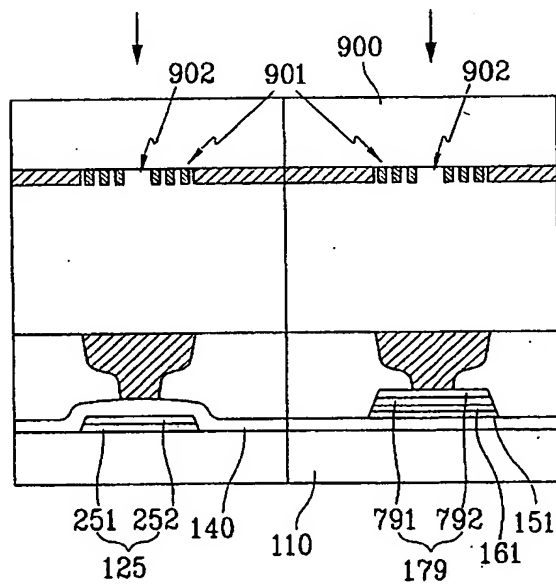


FIG.14

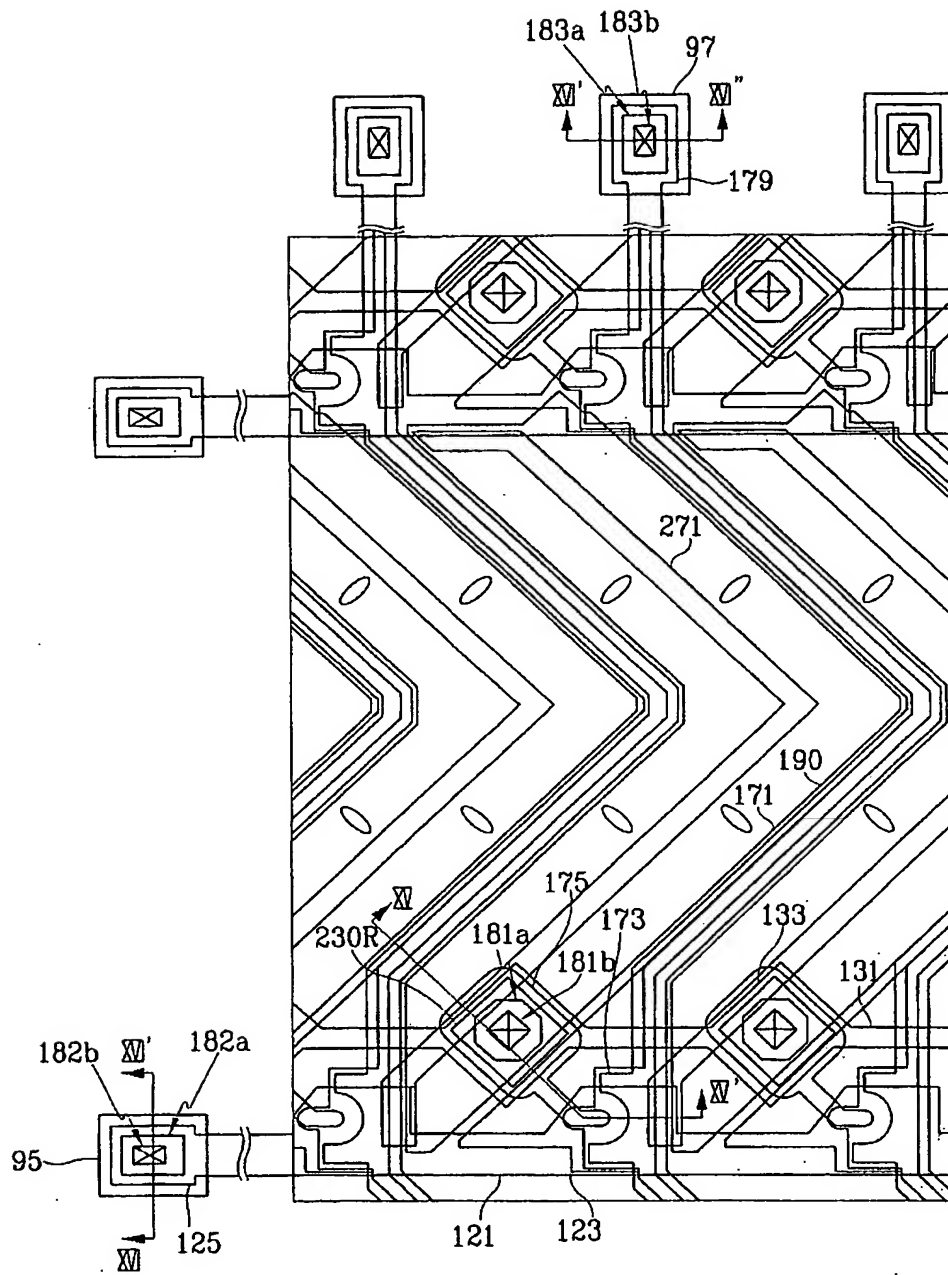


FIG.15

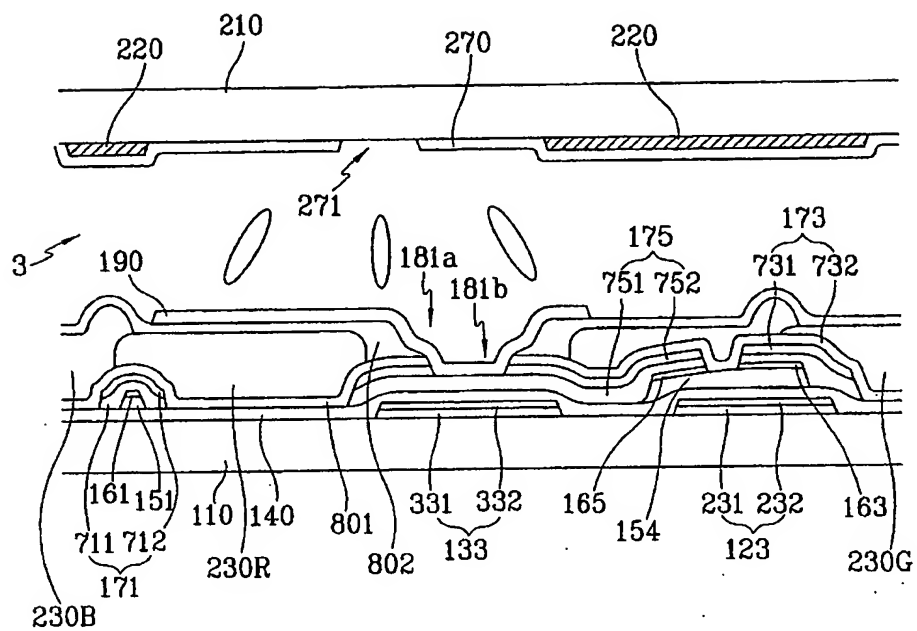


FIG.16

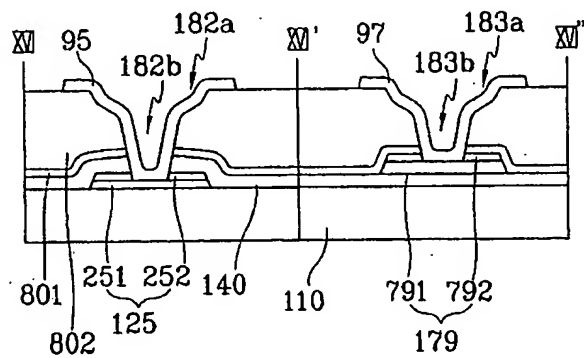


FIG.17

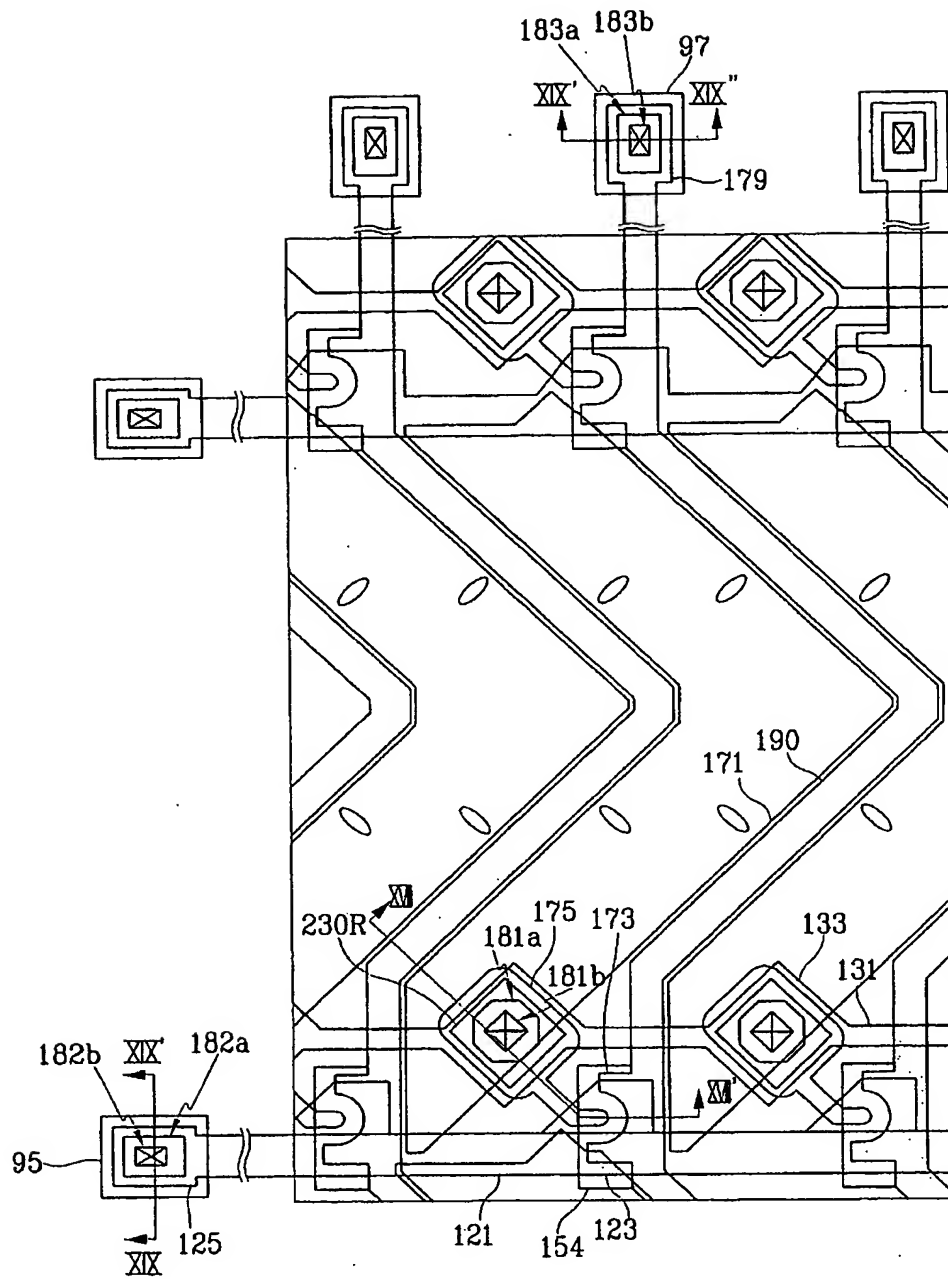


FIG.18

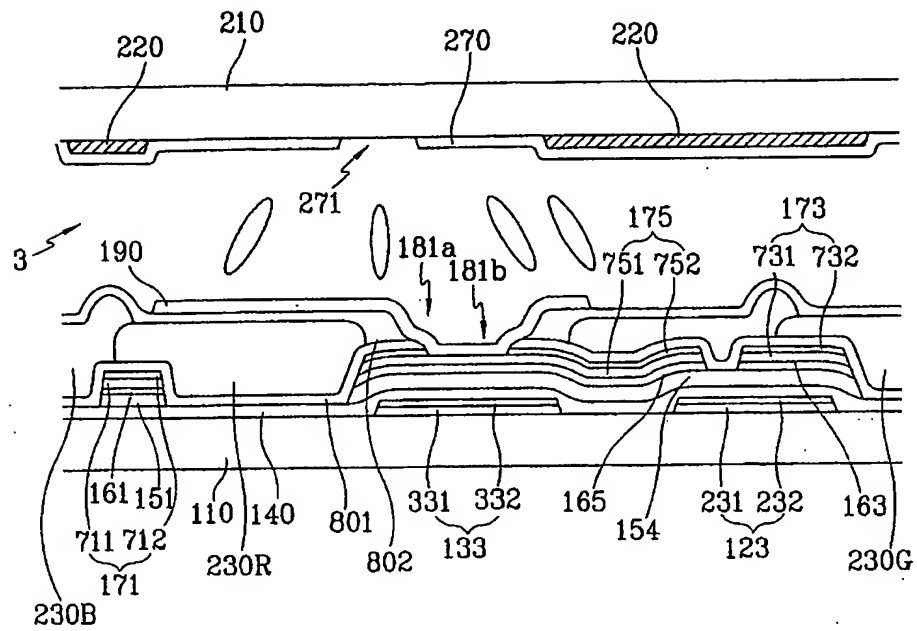


FIG.19

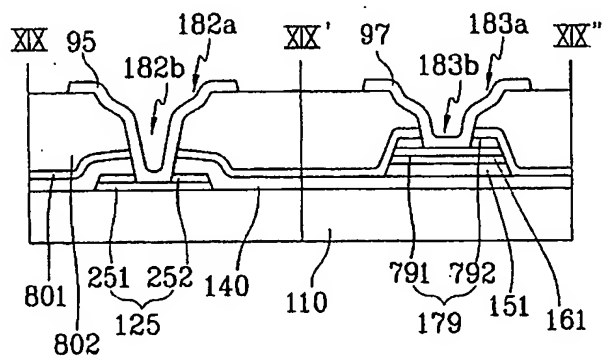


FIG.20

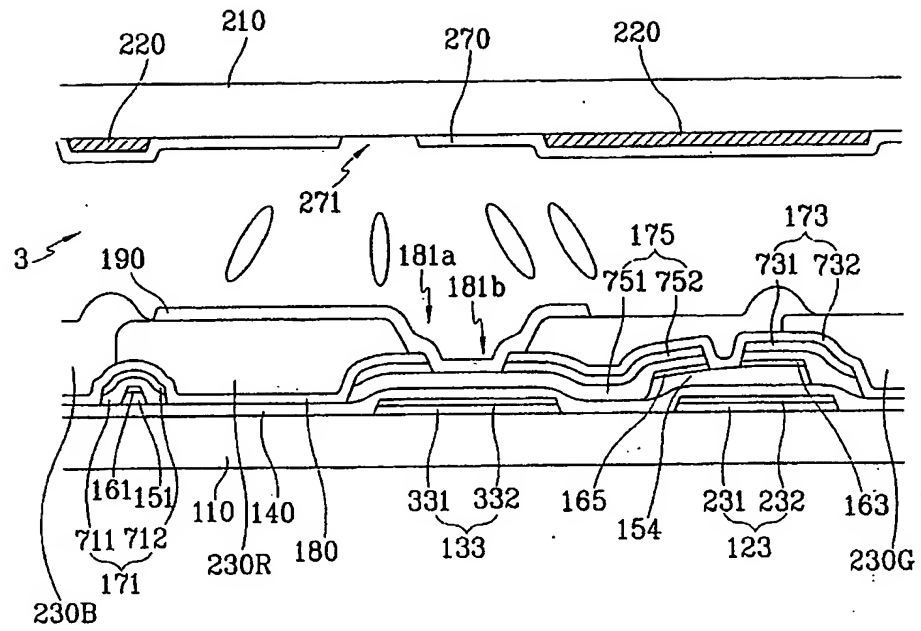


FIG.21

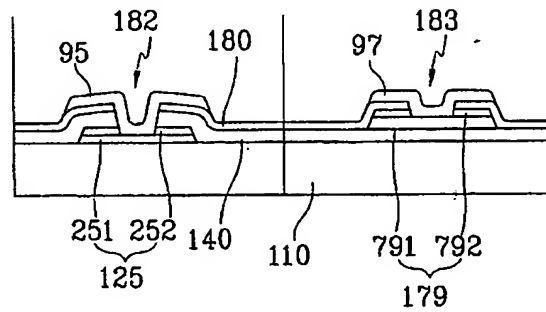




FIG.22

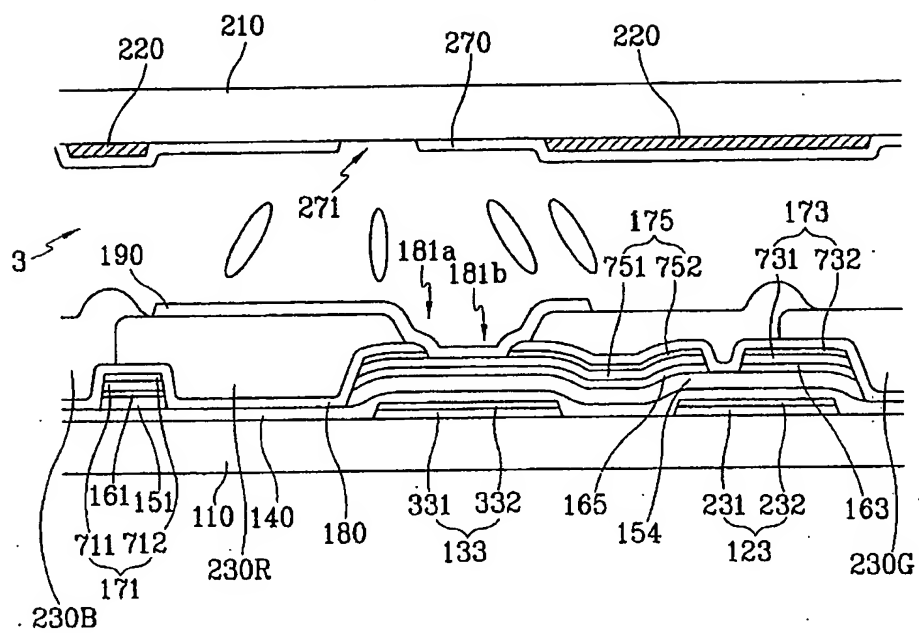


FIG.23

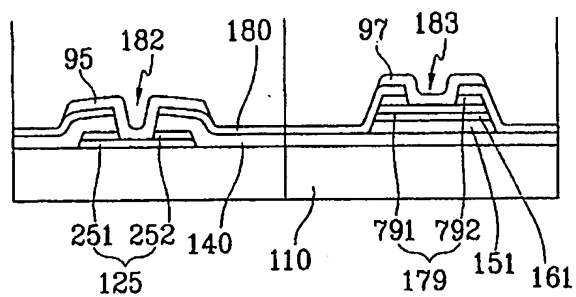


FIG.24

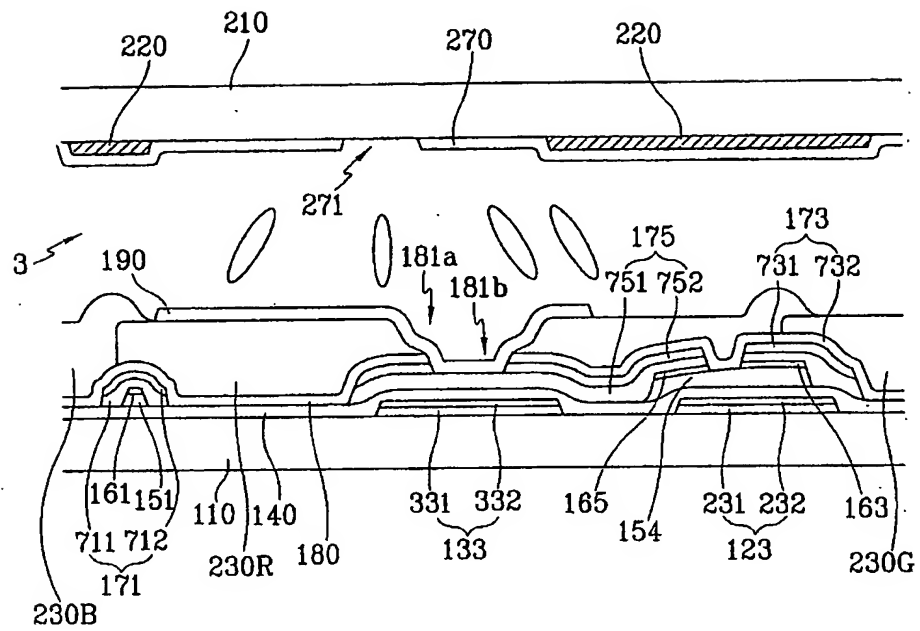


FIG.25

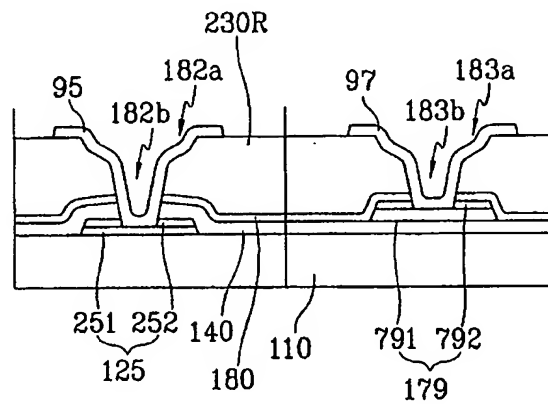


FIG.26

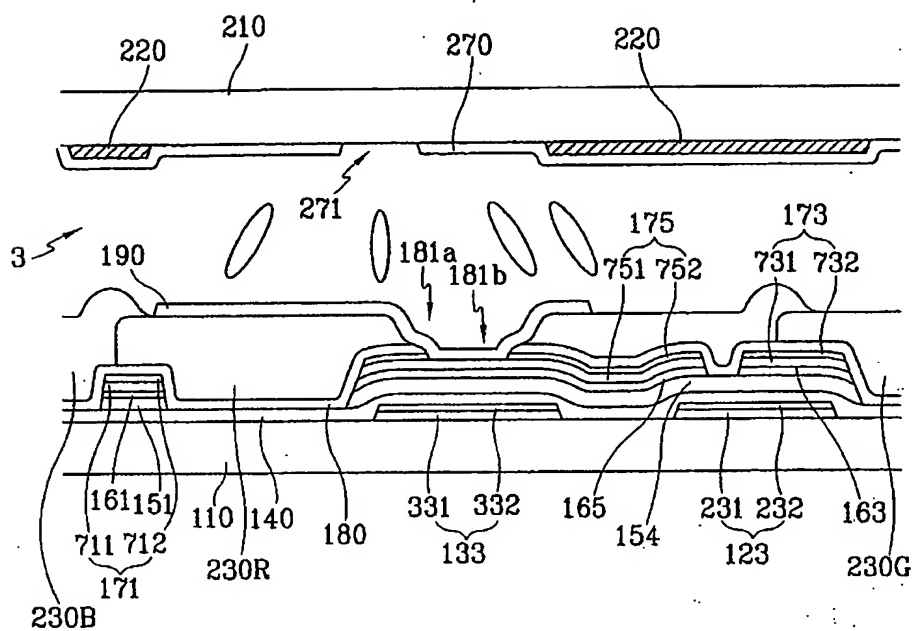


FIG.27

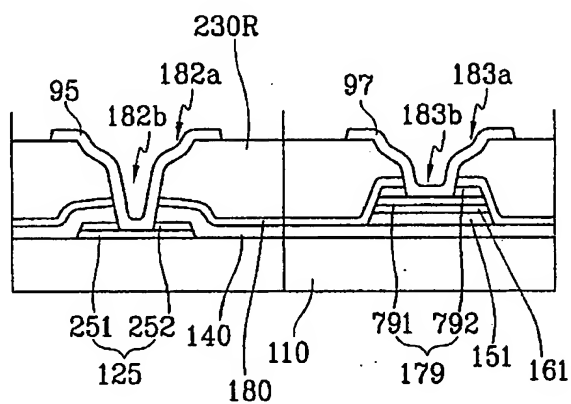


FIG.28

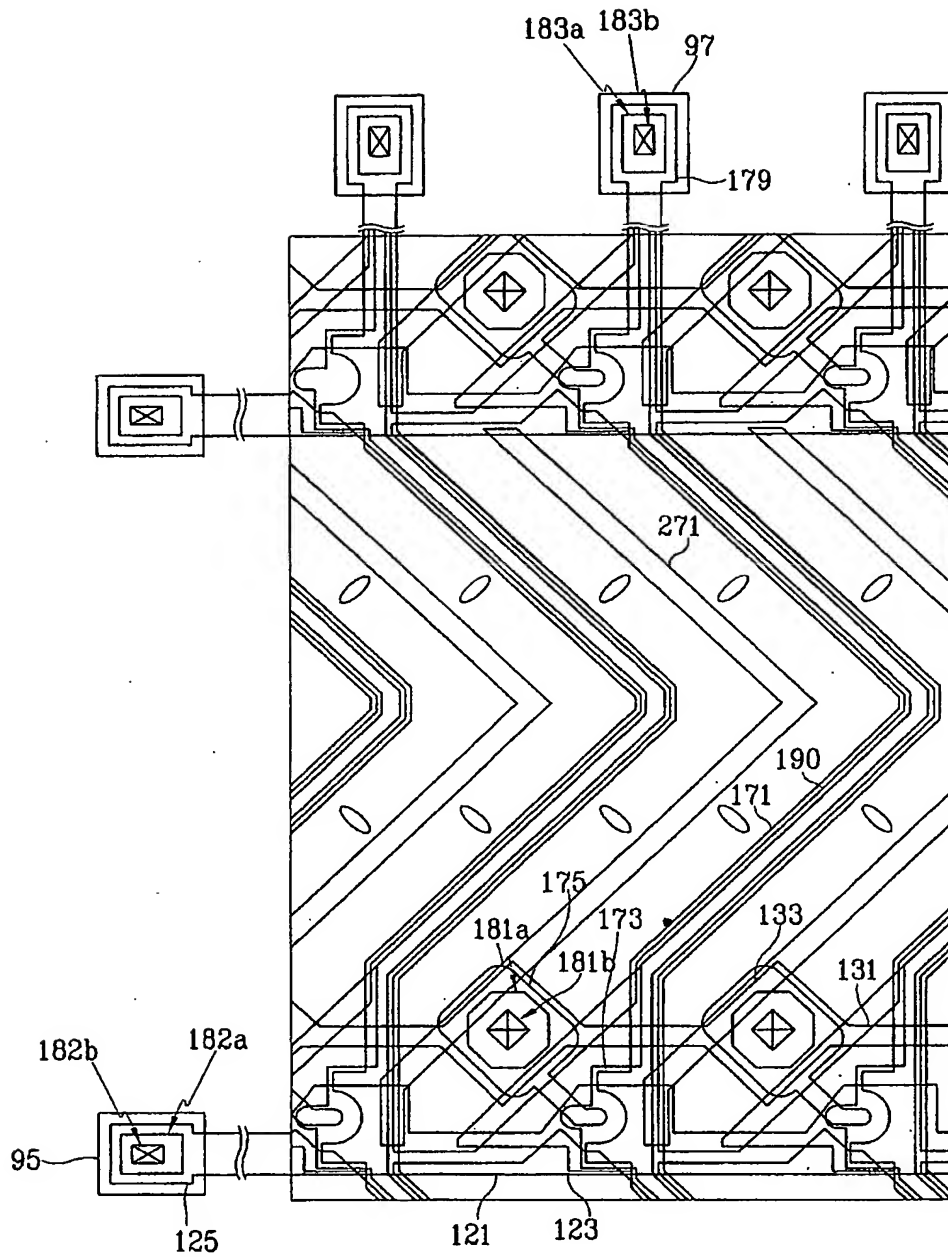


FIG.29

